IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	**O'Donnell**
Application No.	:	**09/961,125**
Filed	:	**September 21, 2001**
For	:	**SCALABLE HOME CONTROL PLATFORM AND ARCHITECTURE**

APPEAL BRIEF

On Appeal from Group Art Unit 2112

Date: July 18, 2005

By: Michael Ure
Attorney for Applicant
Registration No. 33,089

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Shannon Lester
(Name)

(Signature and Date) 7/18/05

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I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the present application, Koninklijke Philips Electronics N.V., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-30 have been presented for examination. All of these claims are pending, stand finally rejected, and form the subject matter of the present appeal.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendment after final rejection has been submitted.

V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates to a scalable home-control platform and architecture suitable to accommodate a wide variety of exiting and future applications. A system view of such a platform/architecture is shown in Figure 3, integrating both legacy and current-generation device and applications. The hardware architecture of such a system is

illustrated in Figure 1, in which a different types of modules, including processing modules (110), control modules (120) and ancillary modules (130) connect to a "backplane" of separate serial buses 150. A typical control module 120 is illustrated in Figure 2. The hardware architecture of such a system is illustrated in Figure 5.

Figure 4 relates to a filter architecture useful for media-processing-type applications.

Independent claim 1 relates to home control platform in which multiple serial buses are configured to provide interconnections among multiple processing units, and a bus allocation control unit configured to receive requests for bandwidth allocation from the processing units, and to provide allocations of subsets of the serial buses to satisfy the requests; wherein the bus allocation control unit aggregates multiple serial buses to satisfy a single request.

Independent claim 22 relates to a processing unit for a home control platform have a filter unit and a bus interface unit. The bus interface unit aggregates multiple serial buses to satisfy a single request.

Independent claim 25 control processor for a home control platform have a central processing unit and a bus interface unit. The bus interface unit aggregates multiple serial buses to satisfy a single request.

VI. GROUNDS of REJECTION to be REVIEWED ON APPEAL

The issues in the present matter are whether:

1. claims 1-4, 8-19, 21 and 25-30 are unpatentable over Zou in view of James; and

2. claims 5-7, 20 and 22-24 are unpatentable over Zou in view of James and further in view of Brotz.

VII. ARGUMENT

I. Rejection of Claims 1-4, 8-19, 21 and 25-30 as unpatentable over Zou in view of James

With respect to Zou, the multiple 1394 buses 30a-f of Figure 1A are point-to-point. As recognized in the Final Rejection, there is not teaching or suggestion in Zou of aggregating multiple serial buses to satisfy a single communication request as currently recited.

However, the Final Rejection states: "James et al. teaches a controller (IRM) in a home network that aggregates multiple serial buses to satisfy a single bandwidth request (Column 9 lines 22-32). It would have been obvious....

The cited portion of James reads as follows:

> Still referring to FIG. 9, a block diagram of one embodiment for adjusting bandwidth that allocates isochronous data traffic on interconnected data buses is shown. Bandwidth adjustment messages do not require any additional routing tables, since the messages flow through bus bridges in the same manner that communication connections are initially established. Furthermore, bus bridge portals need no modification to handle bandwidth adjustment requests, since the requests are handled by controllers.

> The oPCR [outbound portol control register] of talker 1002 indicates the current bandwidth allocated for isochronous data on the talker 1002 bus. The oPCR is updated to reflect the new bandwidth.

In Figure 9 of James, "T" designates a "talker" node, "L" designates a "listener" node, and "C" designates a "controller" node. Three bus bridges are shown, including one bus bridge having elements 1012a-c and one bus bridge having elements 1002a-b. The nodes and bridges are interconnected by 1394 buses. A bold line from talker 1002 to listern 1004 indicates a communicating path between these nodes.

There is absolutely no teaching or suggestion found in the cited portion of James, or elsewhere, of a bus allocation control unit that aggregates multiple serial buses to satisfy a single request, as claimed.

Accordingly, the combination of Zou and James cannot be said to render obvious the invention recited in claim 1.

Claims 25 is believed to patentably define over Zou in view of James for similar reasons.

With regard to dependent claims 2-4, 8-19, 21 and 25-30, these claims depend from independent claims 1 and 25, respectively, which have been shown to be patently distinguishable over the cited reference. Accordingly, these claims are also patently distinguishable and allowable over the cited references by virtue of their dependency upon an allowable base claims.

In view of the above, applicant submits that all of the above referred-to claims are patentable over the teachings of the cited references.

II. Rejection of claims 5-7, 20 and 22-24 as being unpatentable over Zou in view of James and further in view of Brotz

Brotz was cited as purportedly teaching a filter arrangement similar to that claimed. However, Brotz does nothing to remedy the deficiencies of the base combination of Zou in view of James. Hence, claim 22 is believed to patentably define over the base combination further in view of Brotz.

With regard to dependent claims 23 and 24, these claims depend from independent claim 22, which has been shown to be patently distinguishable over the cited reference. Accordingly, these claims are also patently distinguishable and allowable over the cited references by virtue of their dependency upon an allowable base claims.

With regard to dependent claims 2-4, 8-19, 21 and 25-30, these claims depend from independent claims 1 and 25, respectively, which have been shown to be patently distinguishable over the cited reference. Accordingly, these claims are also patently distinguishable and allowable over the cited references by virtue of their dependency upon an allowable base claims.

VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Date: July 18, 2005

By: Michael Ure
Attorney for Applicant
Registration No. 33,089

IX. APPENDIX: THE CLAIMS ON APPEAL

1. A home control platform comprising:

a plurality of serial buses that is configured to provide interconnections among a plurality of processing units,

a bus allocation control unit that is configured to receive requests for bandwidth allocation from the plurality of processing units, and to provide allocations of subsets of the plurality of serial buses to satisfy the requests;

wherein the bus allocation control unit aggregates multiple serial buses to satisfy a single request.

2. The home control platform of claim 1, further including

at least one processing unit of the plurality of processing units.

3. The home control platform of claim 2, wherein

the at least one processing unit includes at least one of:

an MPEG decoder,
an MPEG encoder
a signal processor,
a variable-length decoder,
a variable-length encoder,
a coder-decoder,
a video CODEC,
an audio CODEC,
a Fast-Fourier-Transform device,
a Discrete-Cosine-Transform device,
a video processor, and
an audio processor.

4. The home control platform of claim 2, wherein

the at least one processing unit includes at least one of:

a serial-to-parallel converter,

a parallel-to-serial converter,

a bus arbitrator,

a bus router, and

a direct-memory-access device.

5. The home control platform of claim 1, wherein

the at least one processing unit includes:

a filter unit, and

a SDRAM.

6. The home control platform of claim 5, wherein

the filter unit is configured to be programmable.

7. The home control platform of claim 1, wherein

each of the plurality of serial buses is configured to be self-timing.

8. The home control platform of claim 1, further including

at least one control processor that is configured to provide control of data transfer among the plurality of processing units.

9. The home control platform of claim 8, wherein

the at least one control processor includes at least one of:

a network interface,

a network manager,

a browser, and

a user interface.

10. The home control platform of claim 9, wherein

the at least one control processor includes at least one of:

a serial-to-parallel converter,

a parallel-to-serial converter,

a bus arbitrator,

a bus router,

a protocol stack, and

a direct-memory-access device.

11. The home control platform of claim 8, wherein

the at least one control processor includes:

a bus interface unit, operably coupled to the plurality of serial buses, that is configured to effect transfer of data via the plurality of serial buses, and

a central processing unit, operably coupled to the bus interface unit, that is configured to process input data from the bus interface unit, and is configured to provide processed data to the bus interface unit.

12. The home control platform of claim 11, wherein

the at least one control processor further includes an SDRAM.

13. The home control platform of claim 8, wherein

the at least one control processor further includes

a microkernel that is configured to provide base operating system services that include at least one of:

semaphores,

messaging,

scheduling,

exception management,

task management, and

memory management.

14. The home control platform of claim 13, wherein

the at least one control processor further includes

an interface that is configured to couple the microkernel to a standard operating system.

15. The home control platform of claim 14, wherein

the standard operating system includes one of: Vxworks, WinCE, and LINUX.

16. The home control platform of claim 13, wherein

the task management is configured to provide direct access to at least one of the plurality of processing units,

the at least one of the plurality of processing units being configured as a coprocessor, and

the direct access being provided through a coprocessor interface layer.

17. The home control platform of claim 8, wherein

the at least one control processor is further configured to provide at least one of:

task memory and CPU space isolation,

virus protection, and

money management.

18. The home control platform of claim 8, wherein

the at least one control processor is further configured to provide an interface between the home control platform and at least one legacy consumer product,

the at least one legacy consumer product includes at least one of:

a television,

a telephone,

an audio system,

a video system, and

an appliance.

19. The home control platform of claim 8, wherein

the at least one control processor includes at least one of:

a voice recognition system,

a voice synthesis system, and

a wireless device interface system.

20. The home control platform of claim 1, wherein

each of the plurality of serial buses is configured to be self-timing.

21. The home control platform of claim 1, further including

a power supply that is configured to provide power to one or more of the plurality of processing units.

22. A processing unit for use in a home control platform, comprising:

one or more filter units,

a bus interface unit, operably coupled to a plurality of serial buses of the home control platform, that is configured to:

receive an allocation of a select one or more buses of the plurality of buses from the home control platform, and

provide communication between the home control platform and the one or more filter units via the select one or more buses

wherein, when an allocation of multiple buses is received from the home control platform, the multiple buses are aggregated to satisfy a single communication request.

23. The processing unit of claim 22, wherein

the one or more filter units are configured to effect the function of at least one of:

an MPEG decoder,

an MPEG encoder

a signal processor,

a variable-length decoder,

a variable-length encoder,
a coder-decoder,
a video CODEC,
an audio CODEC,
a Fast-Fourier-Transform device,
a Discrete-Cosine-Transform device,
a video processor, and
an audio processor.

24. The processing unit of claim 22, further including:
a serial-to-parallel converter,
a parallel-to-serial converter, and
a direct-memory-access device.

25. A control processor for use in a home control platform, comprising
a bus interface unit, operably coupled to a plurality of serial buses of the home control platform, that is configured to effect transfer of data via the plurality of serial buses, based on an allocation of a select one or more buses of the plurality of serial buses by the home control platform, and
a central processing unit, operably coupled to the bus interface unit, that is configured to process input data from the bus interface unit, and is configured to provide processed data to the bus interface unit
wherein, when an allocation of multiple buses is received from the home control platform, the multiple buses are aggregated to satisfy a single communication request.

26. The control processor of claim 25, further including
a microkernel that is configured to provide base operating system services that include at least one of:
semaphores,
messaging,
scheduling,

exception management,
task management, and
memory management.

27. The control processor of claim 26, further including
an interface that is configured to couple the microkernel to a standard operating system.

28. The control processor of claim 26, wherein
the task management is configured to provide direct access to at least one of a plurality of processing units,
the at least one of the plurality of processing units being configured as a coprocessor, and
the direct access being provided through a coprocessor interface layer.

29. The control processor of claim 25, further including:
an interface between the home control platform and at least one legacy consumer product, wherein
the at least one legacy consumer product includes at least one of:
a television,
a telephone,
an audio system,
a video system, and
an appliance.

30. The control processor of claim 25, further including at least one of:
a voice recognition system,
a voice synthesis system, and
a wireless device interface system.

X. APPENDIX: RELATED PROCEEDINGS

NONE

XI. APPENDIX: EVIDENCE

NONE